

FIG. 1
 (PRIOR ART)

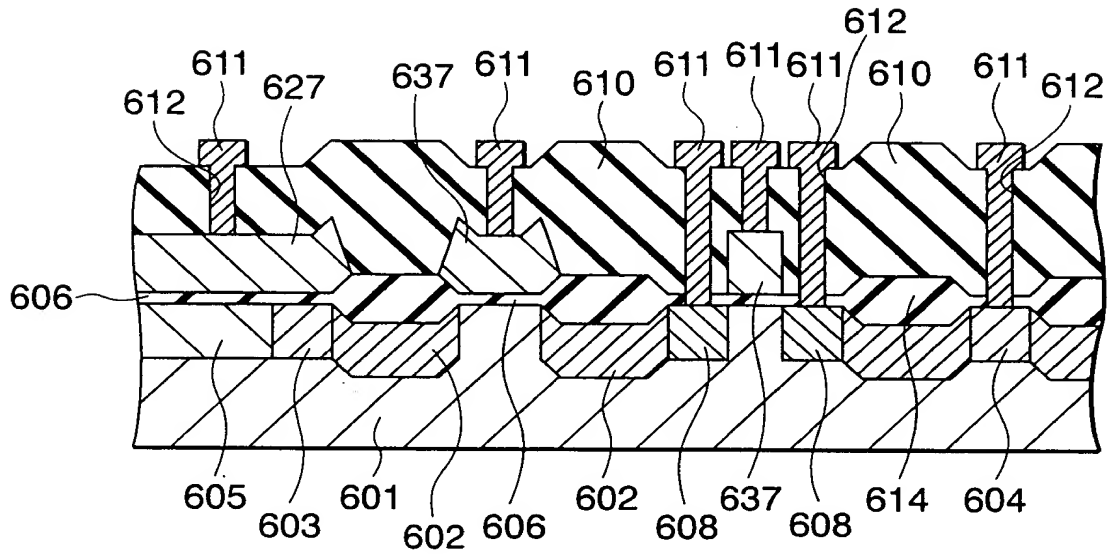


FIG. 2A
 (PRIOR ART)

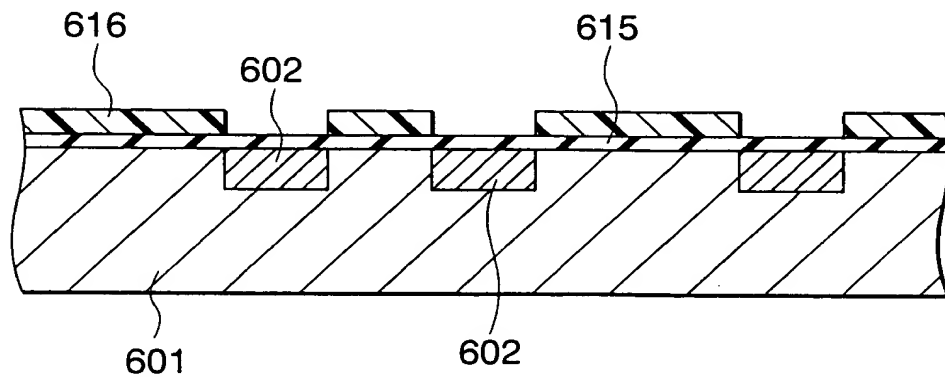
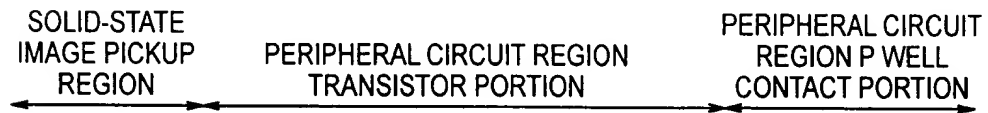


FIG. 2B
(PRIOR ART)

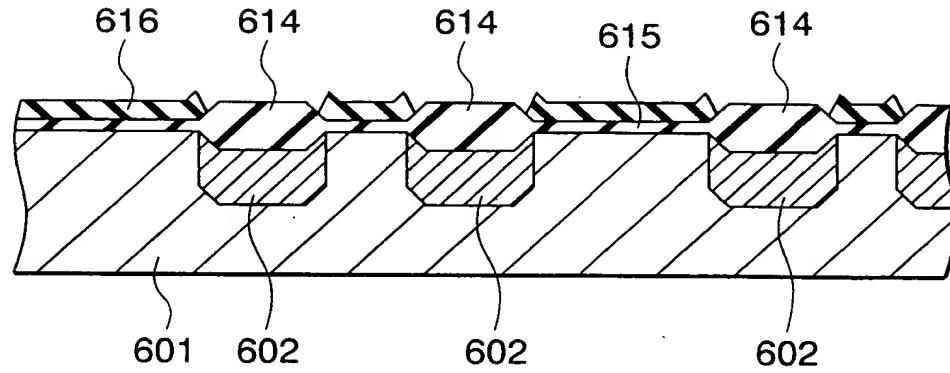
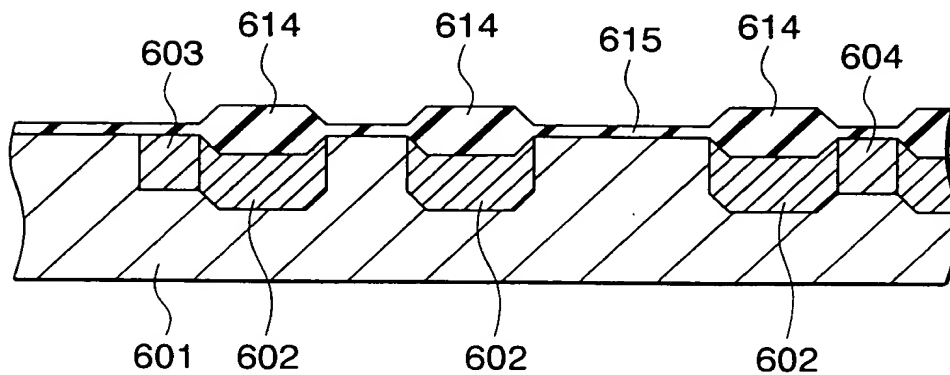


FIG. 2C
(PRIOR ART)



The diagram shows a horizontal line with three distinct regions labeled above it. From left to right, the regions are: SOLID-STATE IMAGE PICKUP REGION, PERIPHERAL CIRCUIT REGION TRANSISTOR PORTION, and PERIPHERAL CIRCUIT REGION P WELL CONTACT PORTION. The regions are separated by vertical lines, and the entire structure is enclosed in a rectangular frame.

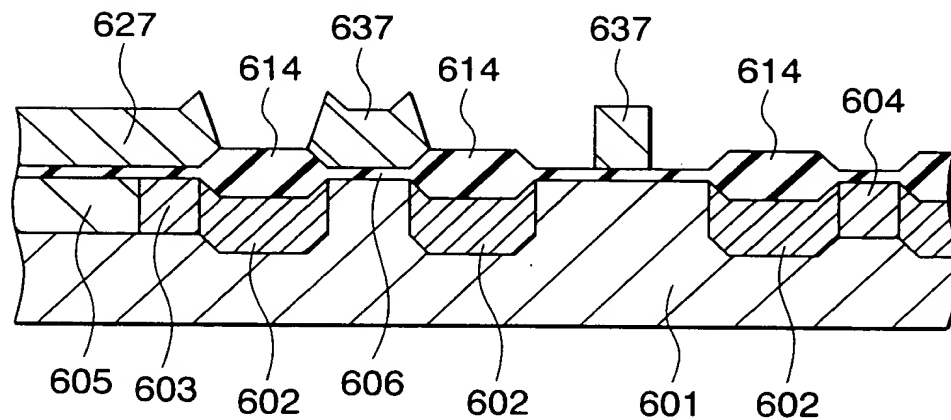


FIG. 2F
(PRIOR ART)

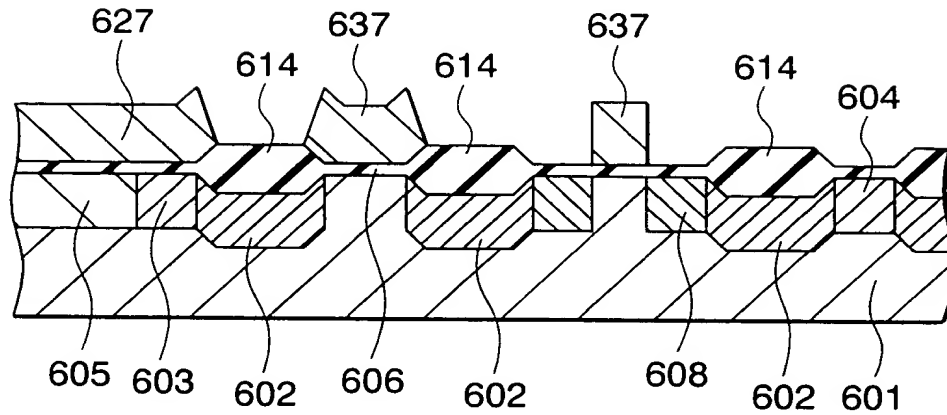


FIG. 2G
(PRIOR ART)

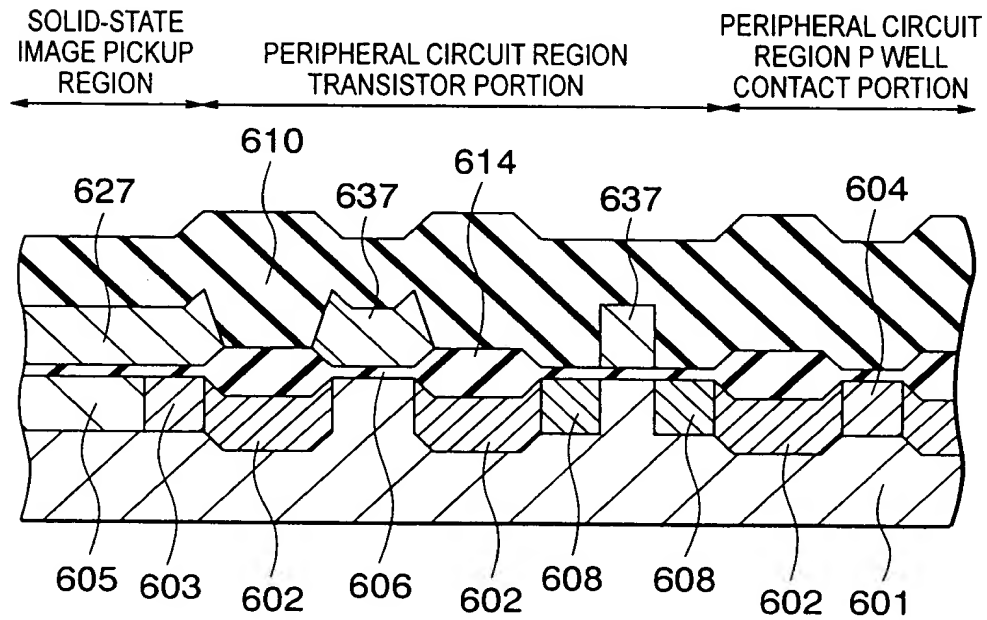


FIG. 2H
 (PRIOR ART)

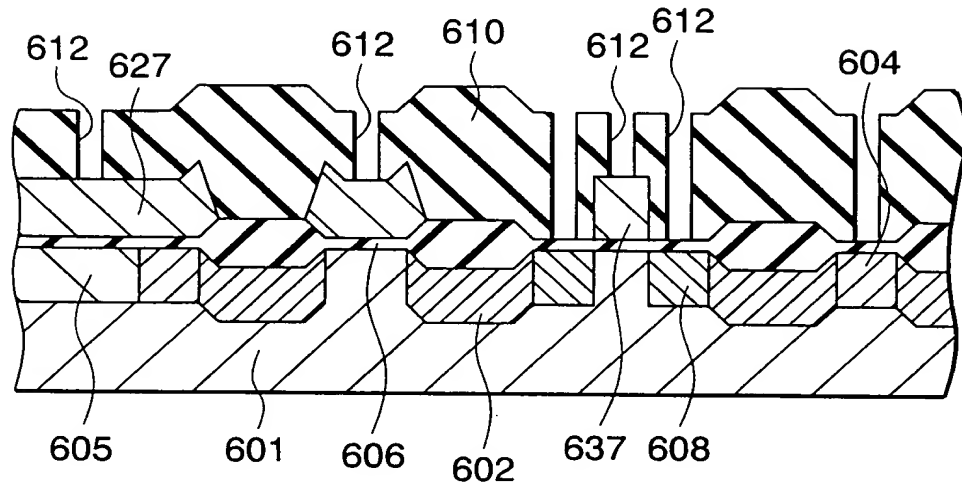


FIG. 3

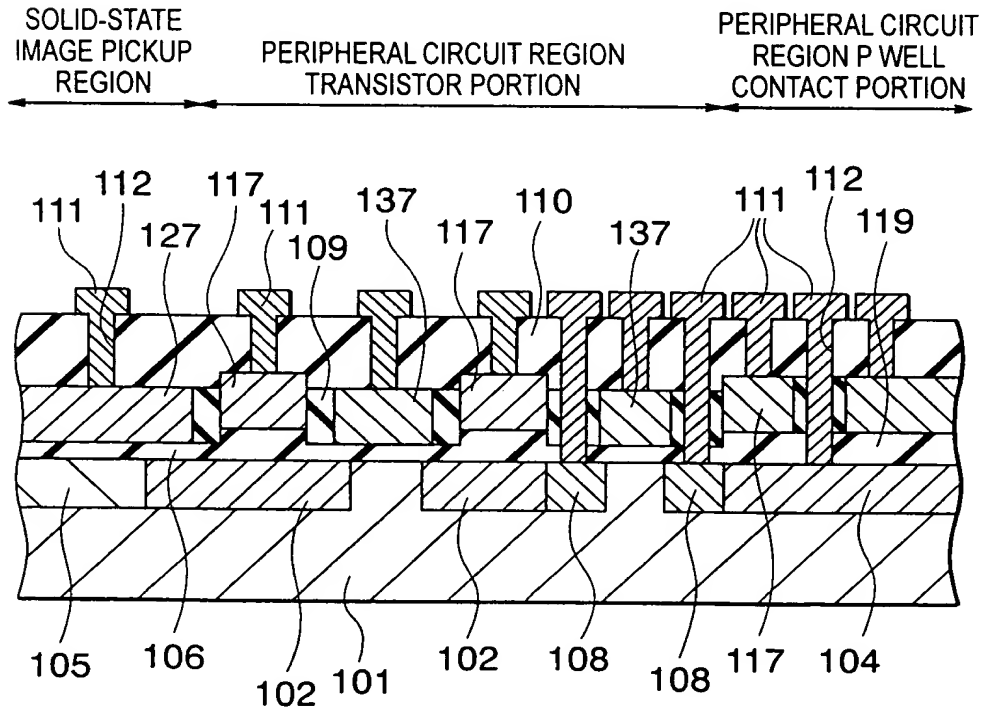


FIG. 4A

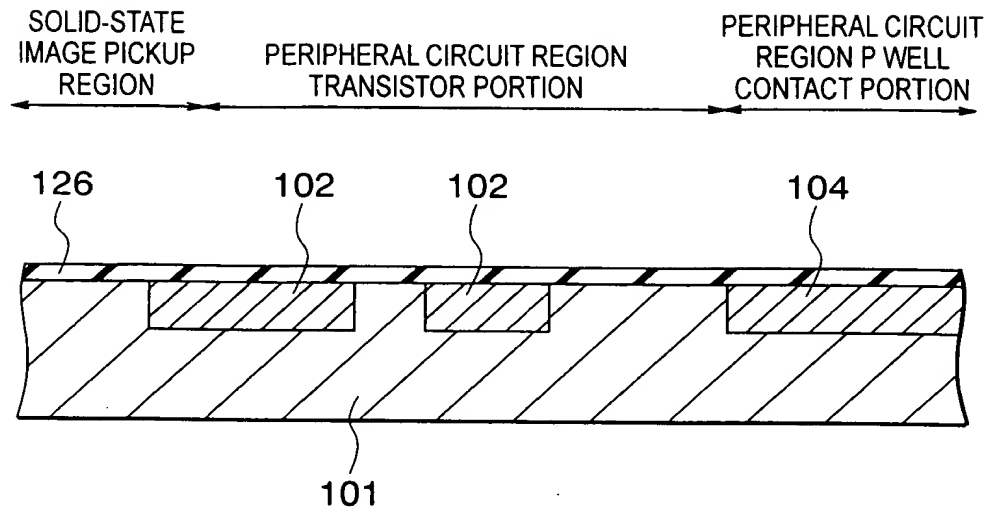


FIG. 4B

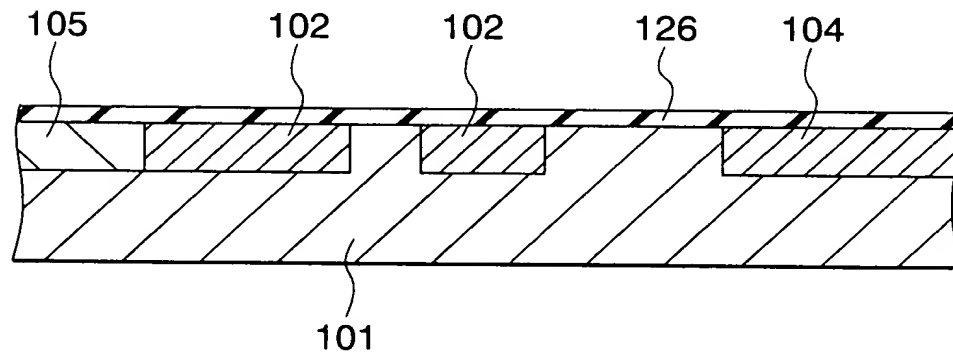


FIG. 4C

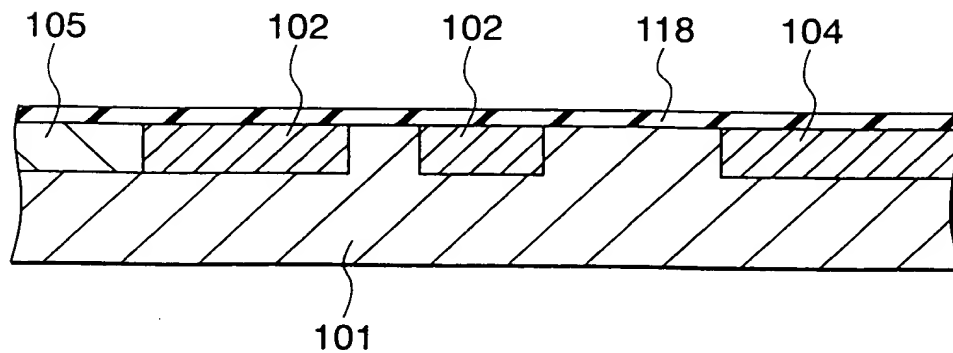


FIG. 4D

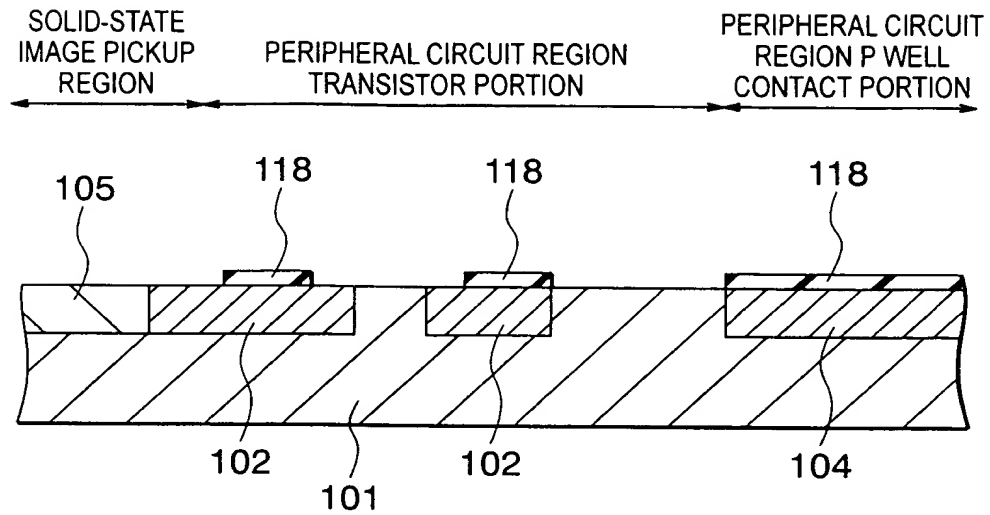


FIG. 4E

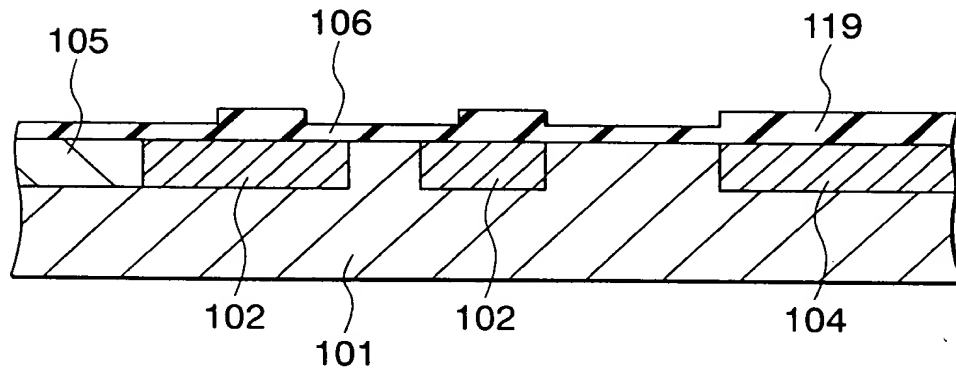


FIG. 4F

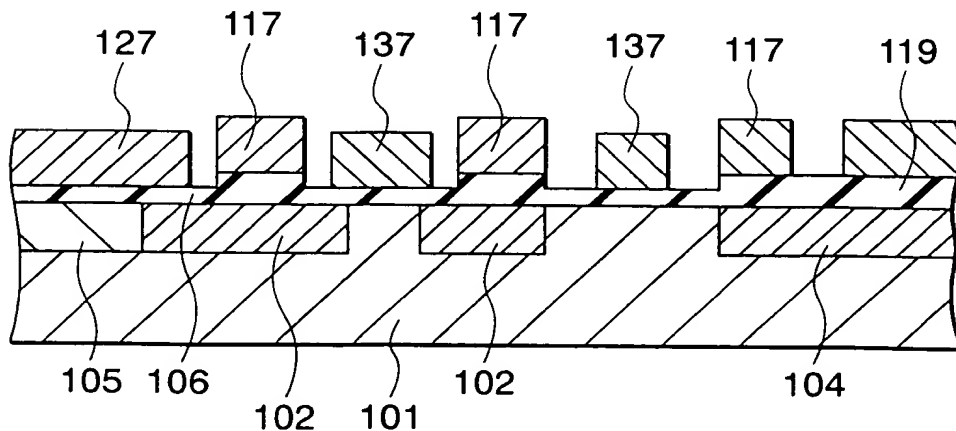


FIG. 4G

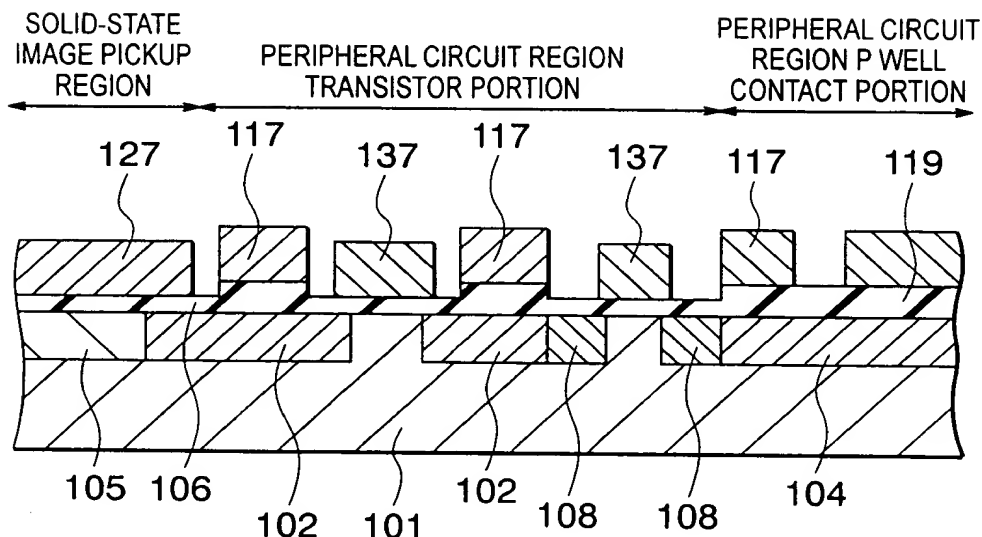


FIG. 4H

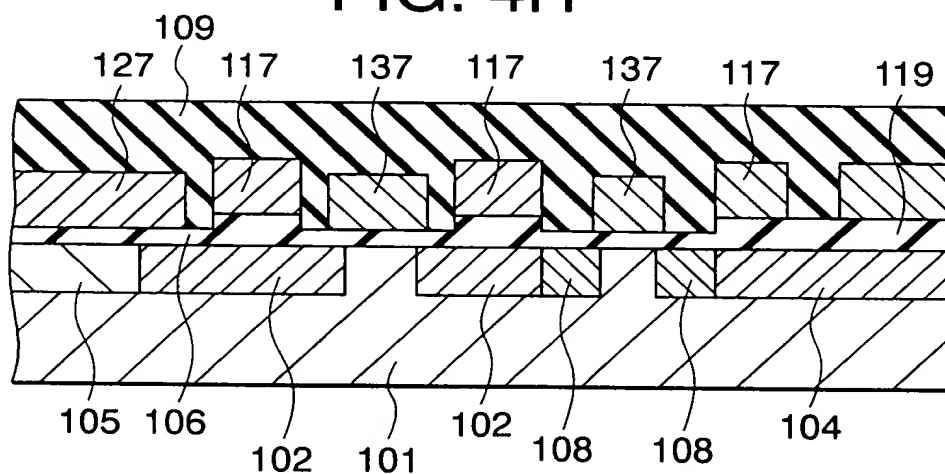


FIG. 4I

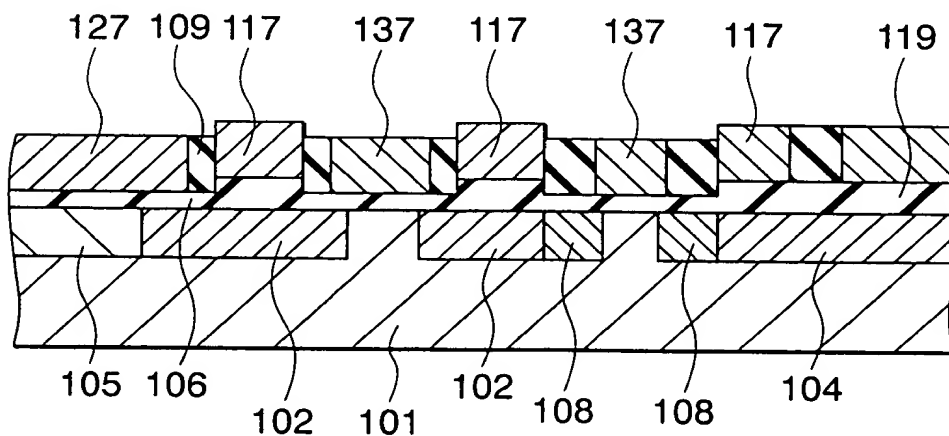


FIG. 4J

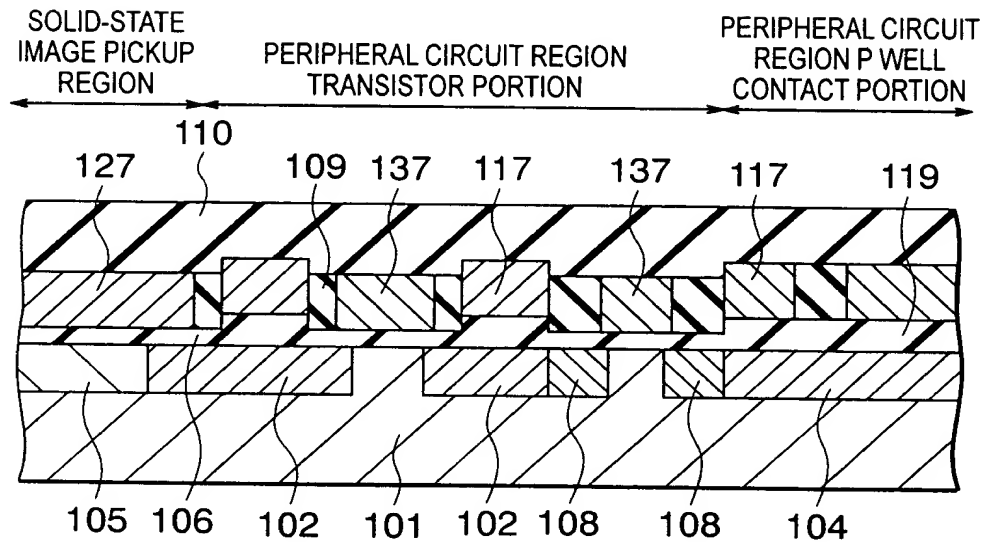


FIG. 4K

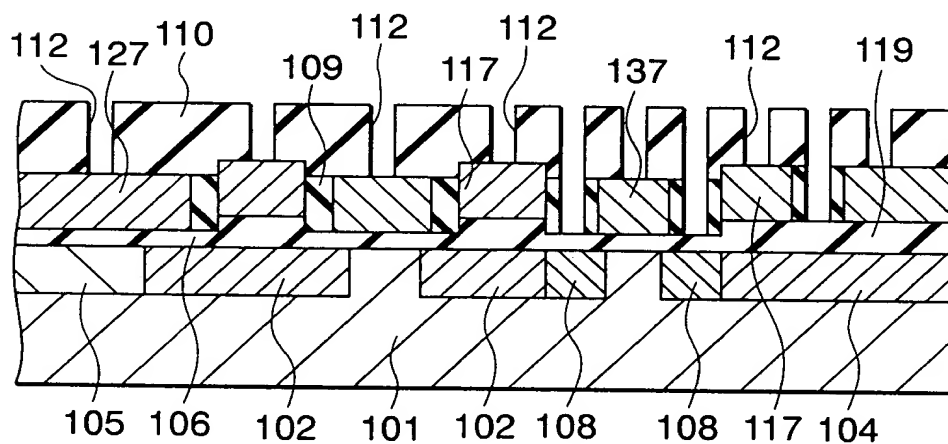


FIG. 4L

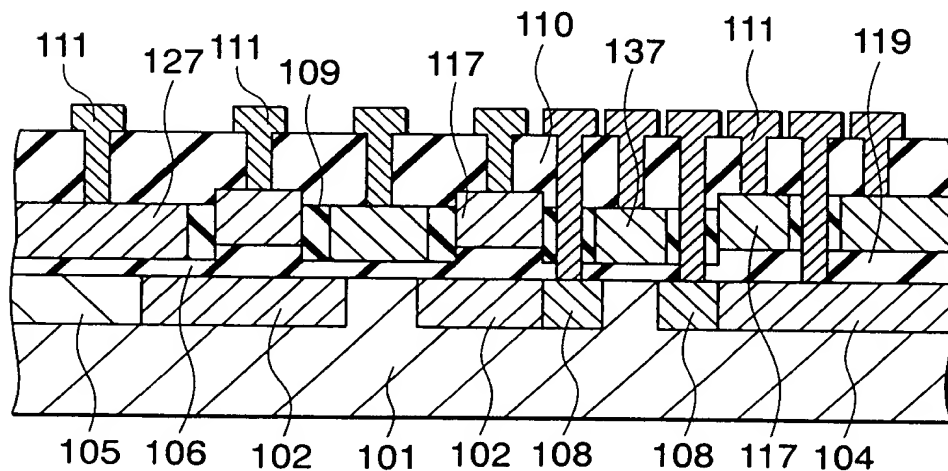


FIG. 5

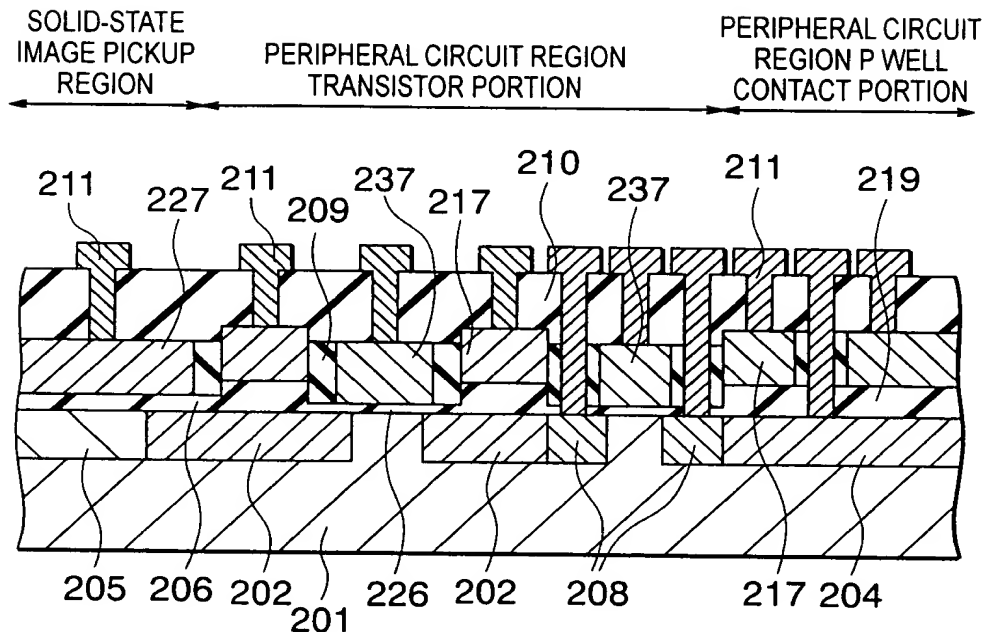
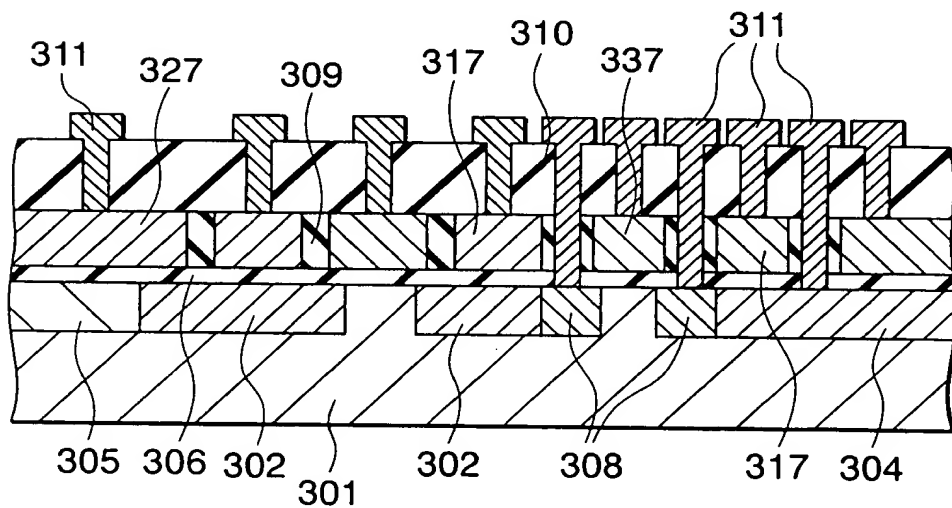


FIG. 6



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